REMARKS

Please reconsider the application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the application.

Disposition of Claims

Claims 4, 16, and 27 are pending in the present application, and claims 4, 16, and 27 are independent. By way of this reply, claims 4, 16, and 27 have been amended to clarify the claim language. Specifically, the claim phrase a "fault location list" has been introduced to better identify what the claimed subject matter is intended for. No new matter has been added by this reply, as support for the amendments can be found in paragraphs [0170]-[0171] of the published specification and Figure 14.

Rejection(s) Under 35 U.S.C § 103

Claims 4, 16, and 27 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,043,672 ("Sugasawara"). To the extent that the rejection still applies to the amended claims, this rejection is respectfully traversed.

One or more embodiments disclosed in this application are directed to a method and apparatus for fault analysis of integrated circuits. In accordance with one embodiment shown in Figures 14 and 15, a circuit to be tested has logic gates **G1, G2, G3, G4, G5**. When the test pattern sequence **T2** (shown in Figure 15, consisting of test patterns "010" and "011") is applied to the circuit, switching operations are expected to be made in the gates **G2, G3, G4, G5**. Therefore, if there is found error in test results when the circuit is tested by applying the sequence **T2**, it should be presumed that one or more of the gates **G2, G3, G4, G5** have defects.

As such, a fault location list *for* the test pattern sequence **T2** is generated as GT2={G2, G3, G4, G5} (*see* paragraphs [0170]-[0171] of the published specification). Similarly, a fault location list for the test pattern sequence **T4** is generated as GT4={G2} (*see* paragraph [0173] of the published specification).

Advantageously, such fault location lists can be employed in testing circuits to easily find where defective elements are located. For instance, according to the embodiments shown in Figures 14 and 15, when test results are detected abnormal in applying the test pattern sequences **T2** and **T4**, the gate **G2** is presumed to a fault location (*see* paragraph [0173] of the published specification).

Accordingly, amended independent claims 4, 16, and 27 require, in part, "storing a fault location list *for the test pattern sequence*, wherein the fault location list includes one or more locations of components in said IC, and the electric potentials at the one or more locations are expected to change when *the test pattern sequence* is supplied" and "presuming a fault location out of said fault location list, *based on said test pattern sequence*, where the transient power supply current shows abnormality, and said fault location list" (emphasis added).

Sugasawara is directed to a test apparatus that introduces dedicated power lines to each region of interest on an IC in order to isolate defects. With respect to Sugasawara, the Examiner asserts in the Advisory Action dated May 5, 2008 that "presuming a fault location" can be seen as the splitting of sections and taking assumptions to isolate power abnormalities as recited in Sugasawara. However, Applicant respectfully notes that a fault location is presumed, based on a test pattern sequence and fault location list in the claimed invention. Specifically, as explained above regarding embodiments according to the claimed invention, a fault location list is generated *for a test pattern sequence*, and a fault location is presumed, based on *the test*

pattern sequence and the fault location list corresponding to *the test pattern sequence*. This is because a fault location list contains locations in the circuit to be tested, where electric potentials are expected to change when *a particular test pattern sequence* is supplied to the circuit.

In contrast, Sugasawara does not teach or suggest such concept of fault location lists. As is clear to those skilled in the art, Sugasawara's split section in a circuit or predetermined reference values are completely irrelevant to locations in a circuit relating to a particular test pattern sequence. Therefore, Sugasawara fails to show or teach at least the limitations "storing a fault location list *for the test pattern sequence*, wherein the fault location list includes one or more locations of components in said IC, and the electric potentials at the one or more locations are expected to change when *the test pattern sequence* is supplied" and "presuming a fault location out of said fault location list, *based on said test pattern sequence*, where the transient power supply current shows abnormality, and said fault location list," as required by amended independent claims 4, 16, and 27.

In view of the above, Sugasawara fails to show all limitations of independent claims 4, 16, and 27. Claims 4, 16, and 27 are therefore patentable over Sugasawara. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 02008/071003).

Dated: May 30, 2008

Respectfully submitted,

By_____

Thomas K. Scherer
Registration No.: 45,079
OSHA · LIANG LLP
1221 McKinney St., Suite 2800
Houston, Texas 77010
(713) 228-8600
(713) 228-8778 (Fax)
Attorney for Applicant

Attachments